L-BAND INTERNALLY MATCHED Si-MMIC LOW NOISE AMPLIFIER

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ABSTRACT

A Si-MMIC low noise amplifier (LNA), fabricated in conventional 0.8um Bi-CMOS process, was developed. This LNA is monolithically integrated on a low resistive Si substrate with coplanar waveguide (CPW) type matching circuits. At 1.9GHz, noise figure of 2.7dB and gain of 10dB were obtained at 2V / 2mA d.c.supply.

1. INTRODUCTION

In recent years, there is an increasing demand for low production cost as well as high RF performance for RF front-end used in cellular handset terminals. In spite of relatively high production cost comparing with Si-MMICs, GaAs-MMICs have been widely employed because of their high RF performance [1] - [4]. On the other hand, RF performance of Si transistors, especially bipolar junction transistor (BJT), has been rapidly improved and Si-MMICs have competitive features with GaAs-MMICs up to L-band[5]-[8] for use of low noise amplifier (LNA). But most of them needed external matching circuits to extract their best performance. In this paper, an L-band Si-BJT LNA with fully monolithic matching circuits is described. This LNA is fabricated in conventional 0.8um Bi-CMOS process. In order to obtain lower NF and higher gain at low d.c. supply power, the optimum emitter size is chosen. To reduce insertion loss of matching circuits, especially spiral inductor, coplanar waveguide (CPW), with 3.5um thick and 11um wide strip line, is employed. At 1.9GHz, a fabricated internal matched monolithic LNA achieved NF of 2.7dB and gain of 10dB at 2V/2mA d.c. supply.

2. CONFIGURATION

Fig.1 shows the emitter size dependence of NFmin of the fabricated BJT in the 0.8um Bi-CMOS process at 1.9GHz. With 1.2V and 2mA d.c.supply, minimum NFmin of 1.9dB is achieved at emitter size of 0.8um×72 um (mask size).

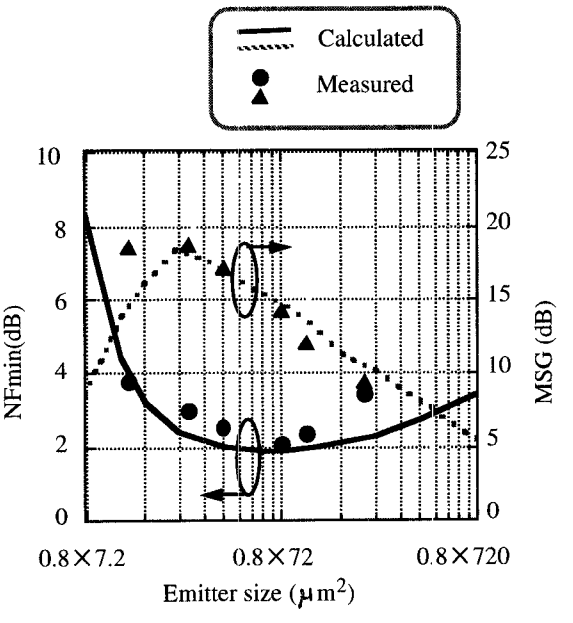

Fig.1 Emitter size dependence of NFmin of the fabricated BJT at 1.9GHz. (Vce=1.2V, Ice=2mA, Calculated data comes from extracted SPICE parameters.)

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Fig.2 shows the schematic diagram of the LNA. Spiral inductors L1 and L2 are used to transform the input / output impedance to 50Ω. In order to reduce dielectric loss due to low resistive Si substrate, CPW is employed. At the same time, to reduce conductor loss, these inductors consist of 3.5um thick and 11um wide aluminum strip line. Since the collector is biased through Rc (= 400Ω), the collector-emitter voltage is 1.2V at supplied d.c. current of 2mA. Fig.3 shows the photograph of fabricated LNA. The chip size is 1mm×2mm, but active area is less than 1mm ×1mm.

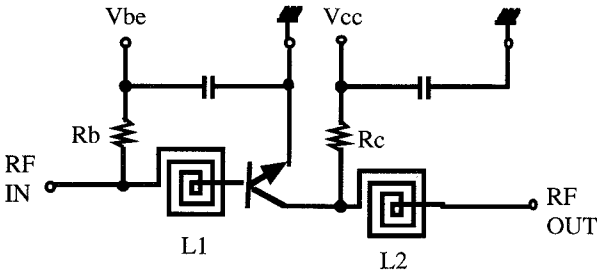

Fig.2 Schematic diagram of the LNA

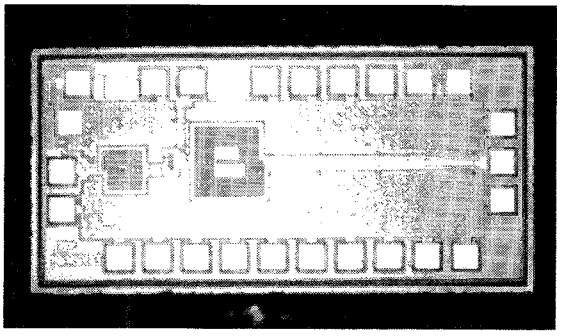

Fig.3 Photograph of the fabricated LNA (Chip size 1mm x 2mm)

3.MEASURED RESULTS

Fig.4 shows the measured frequency dependence of gain and isolation of the fabricated LNA. The d.c. supply condition is 2V/2mA. Gain of 12.8dB is obtained at 800MHz, and 10dB at 1.9GHz. Fig.5 shows the frequency dependence of return loss of the input port and the output ports. The return loss of the input port is less than 5dB due to NF matching, whereas that of the output port is more than 10dB. Because of the low Q of spiral inductor, both ports are matched in broad band. Fig.6 shows the frequency dependence of the noise figure. NF of 2.1dB is achieved at 800MHz, and 2.7dB at 1.9GHz. Fig.7 shows two-tone transfer characteristics at 1.9GHz. Third order intercept point (IP3) is -12.5 dBm at the input port and -2.1 dBm at the output port. Fig.8 shows d.c. supply voltage (Vcc) dependence of gain, noise figure, IP3 at input and output ports. This LNA works sufficient above the Vcc of 1.5V.

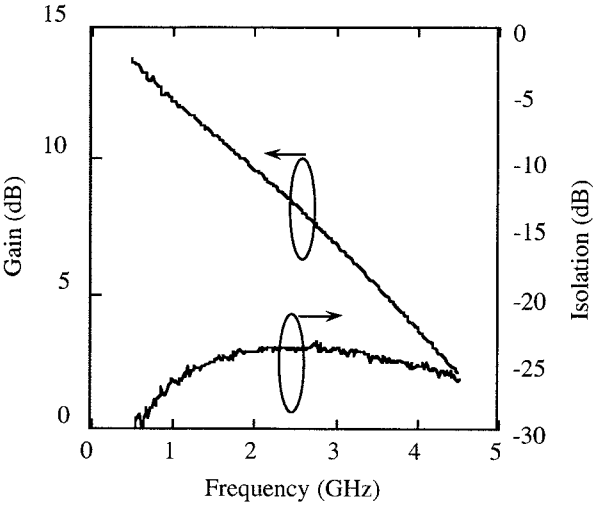

Fig.4 Measured frequency dependence of gain and isolation

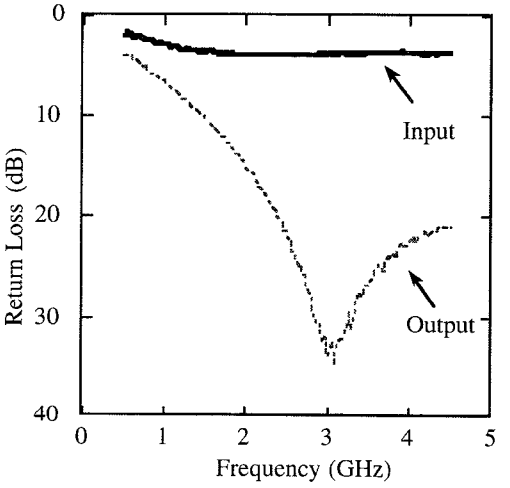

Fig.5 Measured frequency dependence of return loss of input and output ports

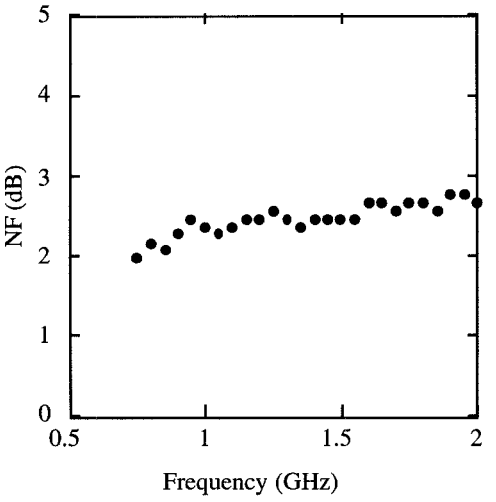

Fig.6 Measured frequency dependence of noise figure

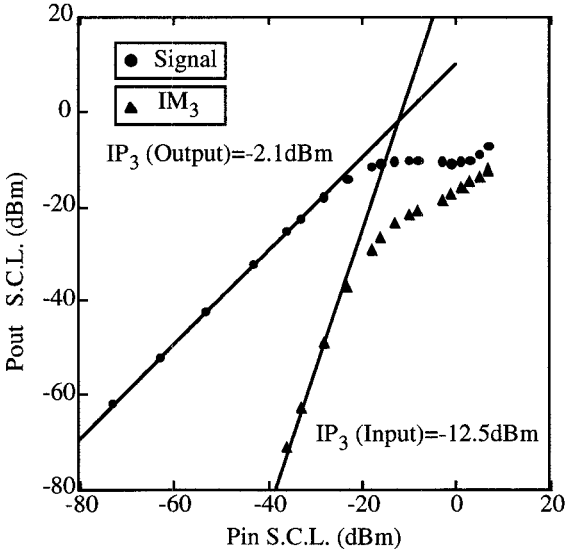

Fig.7 Measured two-tone transfer characteristics at 1.9GHz

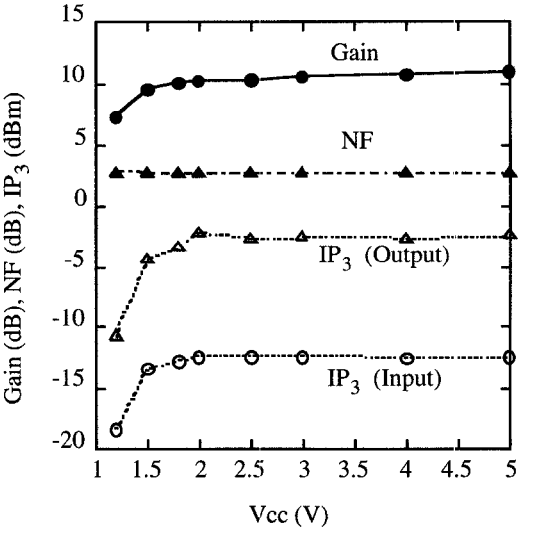

Fig.8 Measured Vcc dependence of gain, noise figure and IP3 (input and output) at 1.9GHz (Ice= 2mA)

4. CONCLUSION

An L-band Si-MMIC LNA with fully monolithic internal matching circuits is developed in conventional 0.8um Bi-CMOS process. By selecting the optimum emitter size of 0.8um×72um, lower NF and higher gain performance can be obtained at extremely low d.c. power supply. By employing CPW with 3.5um thick and 11um wide strip line for matching spiral inductors, monolithic matching circuits with lower insertion loss can be achieved. At 1.9GHz, the fabricated LNA performs NF of 2.7dB and gain of 10dB at 2V/2mA d.c. supply. This LNA could be used as front-end for L-band applications such as mobile communication systems.

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